Short Course

Analog, Mixed-Signal, and RF Circuit Design in Nanometer CMOS

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The relentlessly increasing bandwidths and decreasing costs of high-volume communication systems such as cellular handsets have been enabled by sophisticated digital signal processing techniques made practical by the continued scaling of CMOS technology. However, high-performance analog, mixed-signal, and RF circuitry is also required in these systems, and intense market pressure usually dictates that as much of it as possible be integrated along with the digital circuitry in the same technology. Unfortunately, the design of such circuitry becomes increasingly challenging as CMOS technology is scaled into the nanometer regime (<100 nm); low supply voltages, high 1/*f* noise, high device non-linearity, poor signal isolation, and device leakage limit the effectiveness of traditional analog circuit topologies in critical communication system blocks such as amplifiers, mixers, data converters, and phase-locked loops. This short course will explain the fundamental limitations faced by those designing such blocks in nanometer CMOS, and present state-of-the-art circuit and system-level techniques for addressing these limitations. It is intended for both entry-level and experienced engineers.

OUTLINE

RF Transceiver System Design in Nanometer CMOS

In articles, textbooks and research papers we are told again and again that even as CMOS gate lengths become ever smaller, "the analog doesn't shrink." But cell phones have gotten smaller somehow, and the smart money says they will continue to pack more features in the same or smaller form factor for some time to come. Many of the secrets behind this apparent contradiction lie in the IC system-level design. The RF transceiver designer is faced with myriad design choices that have huge impacts on the overall IC performance. Simply choosing the performance targets for the IC is not to be taken lightly. For example, just as in the digital and traditional mixed-signal domains, a goal of minimizing die area as opposed to minimizing current draw can lead to a vastly different set of choices for the LNA, Mixer, baseband filter, and data converter parameters. Likewise, those ever-shrinking gate lengths do indeed lead one to make sharp turns along the path toward the final block specifications. In this presentation Matt Miller will briefly review the history of transceiver design, which has brought us to the present situation wherein the inclusion of an all-CMOS transceiver in a handheld phone is fast becoming the norm. He will then examine the changes in the CMOS environment - the side effects of all those shrinking gates - that are driving the trend toward digitally assisted and sometimes even disappearing analog circuits, and will show examples of how this trend is making itself felt in the RF arena.

Instructor: Matt Miller received the B.S. degree in electrical engineering from Purdue University in West Lafayette, Indiana in 1987 and the M.S. degree in electrical engineering from National Technological University in 1996. He joined Motorola in 1988 as a member of the Secure Communications Division where he worked on the development of custom integrated circuits for use in encrypted voice radio products. In 1994, he joined Motorola's Communications Research Labs and since that time has been involved in the research and design of mixed-signal and RF integrated circuits with emphasis on data conversion and RF transceivers. He is currently a Distinguished Member of the Technical Staff in the Advanced Technology Group of Freescale Semiconductor. He holds 13 patents, has two patents pending, and is the co-author of five IEEE papers and one AES paper.

RF Circuit Design in Nanometer CMOS

With CMOS technology entering the nanometer regime, the design of analog and RF circuits is complicated by low supply voltages, very non-linear (and non-quadratic) devices and large 1/*f* noise. At the same time, circuits are required to operate over increasingly wide bandwidths to implement modern multi-band communication systems as these systems move toward software-defined radio. These trends in technology and system design call for a re-thinking of analog and RF circuit design in nanometer CMOS. Bram Nauta will discuss innovations intended to enable continued progress in spite of these challenges. These innovations include thermal noise canceling, poly-phase distortion canceling and 1/*f* noise reduction techniques applied to basic RF circuits.

Instructor: Bram Nauta received the M.Sc degree (cum laude) in Electrical Engineering from the University of Twente, Enschede, The Netherlands in 1987. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands, where he worked on high-speed AD converters. From 1994 to 1998 he led a research group in the same department working on "analog key modules." In 1998 he returned to the University of Twente, as full professor heading the IC Design group, which is part of the CTIT Research Institute. His current research interest is high-speed analog CMOS circuits.

Continuous-Time ADCs in Nanometer CMOS

Due to the ever-increasing data rates of wireless communication systems, the ADCs used require ever-increasing bandwidth. Delta-Sigma ($\Delta\Sigma$) ADCs are very popular for applications requiring high-accuracy because their performances are robust with respect to the non-idealities of CMOS technologies. However, because they are usually implemented using switched-capacitor (SC) circuits, their low speeds and aliasing limit their use in telecommunication applications. In addition, $\Delta\Sigma$ ADCs require special techniques in nanometer technologies because of the reduced supply voltages available. Therefore, continuous-time (CT) implementations of $\Delta\Sigma$ ADCs are being investigated for telecommunication applications. Michel Steyaert will present an overview of the differences between CT and SC $\Delta\Sigma$ ADCs and discuss their relative advantages and disadvantages. Jitter issues are important for CT $\Delta\Sigma$ ADCs and will be discussed. Low-sensitivity feedback (V_{ref}) techniques will be described and some design case studies for low-voltage nanometer technologies will be studied.

Instructor: Michel S.J. Steyaert received his Ph.D. degree in Electronics from the Katholieke Universiteit Leuven in June 1987. In 1988 he was an associated assistant professor at UCLA. In 1989 he joined the ESAT-MICAS group at the Katholieke Universiteit Leuven, were he is now a Full Professor and Chair of the Electrical Engineering department. His current research interests are in analog integrated circuits for high-frequency telecommunication systems and high-performance analog signal processing.

Frequency Synthesizers in Nanometer CMOS

Frequency synthesizers are currently an integral part of digital, mixed-signal, and RF system-on-chip solutions. As CMOS processes scale down, raw transistor performance and power consumption dramatically improve on the one hand, but difficulties arise in implementing traditional phase-locked loop architectures on the other hand. In this presentation Robert Bogdan Staszewski will first review these challenges — low-voltage limitations, high gate and off-channel leakage, high flicker noise, highly nonlinear device characteristics, poor isolation from digital logic — and will then summarize some well-known workarounds. He will then focus on recently developed solutions that are usable in nanometer CMOS processes.

Instructor: Robert Bogdan Staszewski received his Ph.D. from the University of Texas at Dallas in 2002 for his research on RF frequency synthesis in digital deep-submicron CMOS. From 1991 to 1995, he worked at Alcatel Network Systems in Richardson, TX. He joined Texas Instruments in Dallas, TX, in 1995 where he holds an elected title of Distinguished Member of Technical Staff for his pioneering work on the Digital RF Processor (DRP) architecture. He is currently a manager of DRP system and design development for transmitters and frequency synthesizers. He has authored and co-authored 60 journal and conference publications and holds 30 issued and 35 pending US patents.

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